

Amendments to the Specification:

Please add the following heading at page 1, line 3:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 USC §119 to German Application No. DE 10305837.0, filed on February 12, 2003, and titled "Memory Module Having a Plurality of Integrated Memory Components," the entire contents of which are hereby incorporated by reference.

FIELD OF THE INVENTION--

Please add the following heading at page 1, line 6:

--BACKGROUND--

Please add the following heading at page 2, line 18:

--SUMMARY--

Please delete the paragraph beginning on page 2, line 23.

Please replace the paragraph beginning on page 3, line 21 with the following amended paragraph:

In one development of the invention, the access control circuit ~~is furthermore~~ can be designed such that, when supplying an access command which has been generated outside

the memory module and indicates the beginning of a memory access, it can receives the command and generates therefrom an access signal sequence for transmission to the selected memory component. The access signal sequence includes at least one activation signal and a subsequent read or write signal. This makes it possible for the memory module to receive only one access command from the memory controller, for example, whereupon the access control circuit generates, within the memory module, an activation signal followed by a read command or write command. This makes possible the need to transmit only one access command between the memory module and a connected memory controller for a memory access. The effective bandwidth of a command bus between the memory module and memory controller is thereby ~~advantageously~~ can be doubled.

Please replace the paragraph beginning on page 4, line 10 with the following amended paragraph:

In one advantageous embodiment of the memory module according to the invention, the access control circuit ~~is~~ can be arranged within a separate semiconductor module on the carrier substrate. In a further embodiment, the memory module ~~is in the form of~~ can be a DIMM module arrangement and the memory components are, in particular, in the form of dynamic random access memories.

Please delete the paragraph at page 4, line 15.

Please add the following heading at page 4, line 17:

--BRIEF DESCRIPTION OF THE DRAWINGS--

Please add the following heading at page 5, line 1:

--DETAILED DESCRIPTION--

Please replace the paragraph beginning on page 5, line 1 with the following amended paragraph:

FIG. 1 illustrates, in a roughly diagrammatic manner, an embodiment of a memory module in accordance with the invention. The present embodiment is a DIMM module arrangement, in the case of which a plurality of integrated memory components, in this case, in the form of DRAM memories 10 to 18 and 20 to 28, ~~are~~ can be arranged on a carrier substrate 50. An access control circuit 30, which is connected to a command and address bus CA and also to a clock signal line CK, is arranged separately from the memory components 10 to 18 and 20 to 28 on the carrier substrate 50. The input-side terminal of the access control circuit 30 ~~is~~ can be connected to the contact strip 40 of the memory module 1. The contact strip has terminals for inputting and outputting data signals DA, terminals for inputting a clock signal CLK and terminals for inputting address signals ADR and command signals CMD. On the input side, the access control circuit 30 ~~is~~ can be connected to the respective terminals of the contact strip 40 for supplying the address signals ADR and command signals CMD. On the output side, the access control circuit 30 ~~is~~ can be connected to a command and address bus CA1 for the first memory rank having the memories 10 to 18 and also to a command and address bus CA2 for the second memory rank having the memories 20 to 28. On the output side, the access control circuit 30 ~~is~~ can be furthermore connected to the clock signal line CK1 for driving the memories 10 to 18 of the first memory rank and to the clock signal line CK2 for driving the second memory rank having the memories 20 to 28. For the purpose of interchanging data, the memories 10 to 18 and 20 to

28 can have respective data terminals DQ10 to DQ18 and DQ20 to DQ28 which may be connected to the data terminals DQ of the memory module 1.

Please replace the paragraph beginning on page 5, line 23 with the following amended paragraph:

As illustrated in more detail by the memory 10, by way of example, the individual memory components can have memory cell arrays having word lines WL for selecting memory cells MC and bit lines BL for reading data signals from, or writing data signals to, the memory cells MC. The memory cells MC ~~are~~ can be arranged in a known manner at crossover points of the word lines WL and bit lines BL and are respectively connected to one of the word lines and one of the bit lines. The memory cells MC each have a selection transistor and storage capacitor (not illustrated). The control input of the transistors ~~being~~ can be connected to a word line WL which activates connected memory cells MC in the event of a memory access.

Please replace the paragraph beginning on page 6, line 8 with the following amended paragraph:

The access control circuit 30 ~~is~~ can be designed such that, when supplying an address signal ADR which has been generated outside the memory module 1, it can receives an address for a memory access to a selected memory component. The access control circuit can ~~respectively~~ generates, from the address ADR received, at least one column address CADR for accessing a bit line BL and row address RADR for accessing a word line WL of the selected memory component, the column address CADR, and row address RADR being transmitted to the selected memory component via the command and address bus CA1, CA2.

The access control circuit 30 ~~furthermore can~~ receives an access command R/W which has been generated outside the memory module 1 (also see FIG. 2 in this respect). This access command indicates the beginning of a memory access. Once this access command has been received, the access control circuit 30 can generates therefrom an access signal sequence having an activation signal ACT and, depending on whether a read or write access is involved, a subsequent read or write command RD or WR for transmission to the selected memory component. One command R/W ~~is therefore required~~ can be used for a read or write access, with the result that the effective bandwidth of the command and address bus CA is can be doubled.

Please replace the paragraph beginning on page 7, line 1 with the following amended paragraph:

In accordance with the multiplex address scheme for a DRAM memory, the column address CADR and row address RADR for accessing a bit line and word line of a selected memory component ~~are~~ can be generated successively in time by the access control circuit 30 for transmission to the selected memory component. In particular, the column address CADR and row address RADR ~~are~~ can be generated such that they are offset by an RAS-CAS delay time tRCD defined by the type of selected memory component.

Please replace the paragraph beginning on page 7, line 7 with the following amended paragraph:

FIG. 2 diagrammatically illustrates an embodiment of an exemplary computer system having a memory controller 4 and a plurality of memory modules 1 and 2 constructed in accordance with the invention. The memory controller 4 ~~is~~ can be connected to a

transmission bus 5. Both ~~being~~can be situated on a so-called motherboard 3 of the computer system. The DIMM modules 1 and 2 ~~are~~can be connected to the transmission bus 5 via plug connectors. The clock signal CLK, address signals ADR, command signals CMD, data signals DA and the access command R/W ~~are~~can be transmitted to the DIMM modules 1 and 2 on the transmission bus 5.

Please replace the paragraph beginning on page 7, line 15 with the following amended paragraph:

For a memory access, only the access command R/W, i.e., either a read or write command, ~~is~~can be transmitted, together with the full address ADR (n bits), from the memory controller 4 to the modules 1 and 2. The respective access control circuit 30 on the modules 1, 2 can undertakes the DRAM-specific address multiplexing. This means that a row address RADR (r bits), together with an activation signal ACT, and subsequently a column address CADR (c bits), together with a read or write command RD, WR, ~~are~~can be generated and transmitted to the selected memory component. In this case, $n = r + c$, it generally being the case that $r > n/2 > c$. The resulting unburdening of the memory controller 4 ~~makes it possible to~~can reduce the design complexity of the latter. In addition, the access control circuit 30 ~~advantageously enables decoupling between~~can decouple the transmission bus 5 of the motherboard 3 and the communication buses within the module. This makes it possible, for example, to operate the transmission bus 5 between the memory controller and DIMM modules at a higher data rate than the communication buses within the module.

Please insert the following paragraph at page 8, line 6:

A number of implementations have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope. Accordingly, other implementations are within the scope of the following claims.